AMENDMENTS TO THE SPECIFICATION

Please replace paragraph [0041] on page 12 with the following:

[0041] In accordance with process segment 160, the glass 58 backbone [[66]] is subsequently annealed to drive off selenium from the silver-germanium-selenide glass and form a more rigid glass structure. Next, according to process segment 170, a second metal electrode 54 is formed in contact with the silver-germanium-selenide glass 58.

On page 13, please replace paragraph [0044] with the following:

[0044] The first electrode 52 may also be electrically connected to a source/drain region 81 of an access transistor 83, which is fabricated within and on substrate 62. Another source/drain region 85 may be connected by a bit line plug 87 to a bit line of a memory array. The gate of the transistor 83 may be part of a word line which is connected to a plurality of resistance variable memory elements just as [[the]]a bit line [[93]] (not shown) may be coupled to a plurality of resistance variable memory elements through respective access transistors. The bit line [[93]] may be formed over a fourth insulating layer [[91]] (not shown) and may be formed of any conductive material, for example, a metal. ~~As shown, the~~The bit line [[93]] connects to the bit line plug 87, which in turn connects with access transistor 83.

On page 13, between paragraphs [0045] and [0046], please add the following:

[0045.1] FIG. 3 illustrates a processor system 20 which includes a memory circuit 40, e.g., a memory device, which employs resistance variable memory elements 10 (FIG. 2) according to the invention. The processor system 20, which can be, for example, a computer system, generally comprises a central processing unit (CPU) 22, such as a microprocessor, a digital signal processor, or other programmable digital logic devices, which communicates with an input/output (I/O) device 24 over a bus 30. The memory circuit 40 communicates with the CPU 22 over bus 30 typically through a memory controller.

[0045.2] In the case of a computer system, the processor system 20 may include peripheral devices such as a floppy disk drive 26 and a compact disc (CD) ROM drive 28, which also communicate with CPU 22 over the bus 30. Memory circuit 40 is preferably constructed as an integrated circuit, which includes one or more resistance variable memory elements, e.g., devices 10 (FIG. 1). If desired, the memory circuit 40 may be combined with the processor, for example CPU 22, in a single integrated circuit.

AMENDMENTS TO THE DRAWINGS

The attached sheet(s) of drawings includes changes to FIG. 3.

FIG. 3 has been amended to change the reference numeral "140" to "40."

Attachment: Replacement sheet

Annotated sheet showing changes